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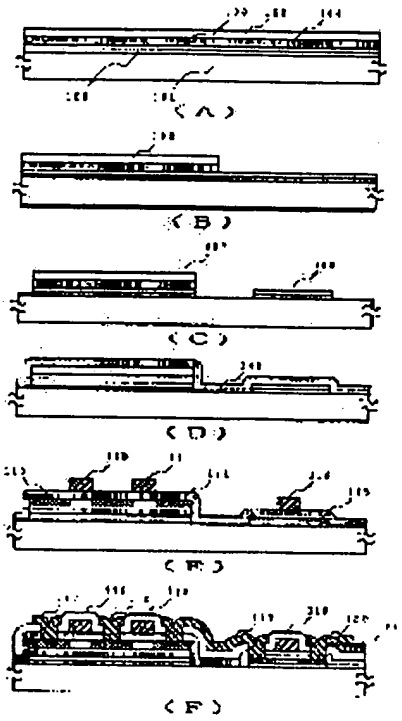
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To control crystallinity and to easily form two types of TFT by altering a process to a minimum limit by specifying a thickness of one active layer and a thickness of an active layer of the other thin film transistor in an integrated circuit having two polysilicon thin film transistors on the same substrate.
CONSTITUTION: A first base oxide film 102 and a first amorphous silicon film 103 are deposited on a substrate 101. A second silicon oxide film 104 and a second amorphous silicon film 105 are deposited on the film 103. Then, a second silicon oxide film 107 and a second amorphous silicon 106 remains only on a peripheral circuit region, and the film 103 is exposed on the other region. An insular region 108 is formed on the exposed part, and crystallized by hot annealing at 450°C. Thus, two types of TFT having a thickness of one active layer of 70nm or less and the other of 70nm or more can be formed.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] this invention relates to an integrated circuit and its production technique. Specifically, like a LCD or a dynamic RAM (DRAM), it has matrix structure, and it has MOS type or MIS (metal-insulator-semiconductor) type electric field effect type element (the above is named MOS type element generically) as a switching element, and is related with the semiconductor circuit which has the matrix equipment (electro-optics display and semiconductor memory equipment are included) characterized by performing a dynamic operation and a drive circuit for it, or an integrated drive circuit like image sensors. Especially this invention relates to the equipment which has the polysilicon contest TFT in which the barrier layer of TFT was formed from contest polysilicon as an MOS type element about the equipment which uses thin-film-semiconductor elements, such as a thin-film-semiconductor transistor formed on the insulating front face.
[0002]
[Description of the Prior Art] Recently, the research of an insulated-gate type semiconductor device which has a thin film-like barrier layer (it is also called an active region) on an insulating substrate is made. Especially, a thin film-like insulated gate transistor and the so-called TFT (TFT) are studied eagerly. These are formed in transparent insulation machine tabular, and in display, such as liquid crystal which has matrix structure, it is the purpose the thing used for a control of each pixel or to use for the drive circuit of image sensors similarly formed in insulation machine tabular, and they are distinguished by the material and the crystallized state of the semiconductor to use like amorphous silicon TFT or polysilicon contest (it is also called polycrystal silicon) TFT.
[0003] But recently, the research also using the material which presents contest polysilicon and the amorphous interval-status is made. Although the argument is made about the interval-status, suppose that all the things that reached a certain crystallized state according to a certain thermal process (for example, irradiate powerful energy, such as heat annealing with a temperature of 450 degrees C or more and laser light) are called contest polysilicon on these specifications.
[0004] Moreover, also in a single-crystal-silicon integrated circuit, as the so-called SOI technique, polysilicon contest TFT is used and this is used as a load transistor for example, in highly-integrated SRAM. However, most amorphous silicon TFT is not used in this case.
[0005] Furthermore, in the semiconductor circuit on an insulating substrate, since there is no capacity coupling of a substrate and a wiring, the extraordinary fast turn around is possible and the technique used [overly] as a high-speed microprocessor or a super-high speed storage is proposed.
[0006] Generally, the electric-field mobility of the semiconductor of the amorphous status is small, therefore cannot be used for TFT as which a fast turn around is required. Moreover, in an amorphous silicon, the electric-field mobility of P type is the parvus remarkably, cannot produce P channel type TFT (TFT of PMOS), therefore cannot form MOS circuit (CMOS) of a complementary type combining N channel type TFT (TFT of NMOS).
[0007] However, TFT formed by the amorphous semiconductor has the characteristic feature of the parvus in OFF current. Then, like the transistor of the active matrix of the parvus liquid crystal display of a matrix scale, so much fast turn around is not demanded, but it is used for the intended use for which high TFT of charge hold capacity is fully needed only by one conductivity type. However, it was difficult for the more advanced application, for example, the liquid crystal display of a large-scale matrix, to use amorphous silicon TFT. Moreover, it has not used for the circumference circuit of a display or the drive circuit of image sensors where a fast turn around is demanded with a natural thing. Moreover, although it is similarly a matrix configuration, it was difficult to also use for semiconductor memory equipment.
[0008] On the other hand, a polycrystal semiconductor has electric-field mobility larger than an amorphous semiconductor, therefore the fast turn around is possible for it. For example, in TFT using the silicon layer which carried out the recrystallization by the laser annealing, 300cm2 / Vs thing value is acquired as electric-field mobility. Since it is a very big value and MOS circuit on single crystal silicon is on an insulating substrate to a working speed being restricted by a substrate and the parasitic capacitance during a wiring, judging from the electric-field mobility of the MOS transistor formed on the usual single-crystal-silicon substrate being 500cm2 / Vs grade, there is such no constraint in any way, and the remarkable fast turn around is expected.
[0009] Moreover, since not only TFT of NMOS but TFT of PMOS is obtained similarly, it is possible to form a CMOS circuit, for example, in the LCD of an active matrix, the thing which constitutes not only an active matrix fraction but circumference

circuits (driver etc.) from the polycrystal TFT of CMOS and which has the so-called monolithic structure is known for contest polysilicon. TFT used for the above-mentioned SRAM also observes this point, constitutes PMOS from TFT, and makes this the load transistor.

[0010] Moreover, in usual amorphous TFT, it is difficult to form the source / drain field according to a self aryne process which is used with single crystal IC technique, and since polysilicon contest TFT can adopt a self aryne process to the parasitic capacitance by the geometric lap of a gate electrode, and the source / drain field posing a problem, a parasitic capacitance has the characteristic feature of being stopped remarkably.

[0011] However, polysilicon contest TFT prepared the supplementary capacity for a leakage current when the voltage is not impressed to the gate (at the time of un-choosing) compensating this leakage current, in order are large and to use it with a liquid crystal display compared with amorphous silicon TFT, TFT is further made into a two step serial, and a means to reduce a leakage current was provided.

[0012] for example, high OFF resistance of amorphous silicon TFT -- using -- in addition -- and if it is going to form the circumference circuit of polysilicon contest TFT which has high mobility monolithic on the same substrate, an amorphous silicon is formed, laser is irradiated alternatively at this, and the technique of making only a circumference circuit crystallize is proposed

[0013] However, since the yield would now use amorphous silicon TFT with low mobility for an active matrix field low from the problems (for example, the homogeneity within a field of irradiation energy is bad) of the reliability of a laser radiation process, more advanced use was difficult. About the laser radiation process, it is more reliable and low heat annealing of a cost was desired. Moreover, as for the mobility of TFT, 2/Vs was desired 5cm also by the minimum from the meaning which raises the value added of a product.

[0014]

[Problem(s) to be Solved by the Invention] such [this invention] a difficult technical probrem -- receiving -- an answer -- it is going to give -- although it is a thing, it is not desirable for a process to be complicated for the reason and to cause a yield fall and cost elevation The place made into the main point of this invention is to make easily and divide two kinds of TFT called TFT as which high mobility is required, and TFT as which a low leakage current is required by change of the minimum process, maintaining mass-production nature.

[0015]

[How to solve a problem] The semiconductor circuit where this invention is applied is not universal. The material from which the permeability of light and reflex nature change with the effects of electric fields, such as a LCD, is used especially for this invention. Insert these materials between the electrodes which counter and the electric field are applied between counterelectrodes. Similarly the MOS structure section of an MOS transistor is used as a capacitor. the active matrix circuit for performing image display, and the memory apparatus which holds storage by accumulating a charge to a capacitor like DRAM -- or to the circuit and pan which have a dynamic circuit like the dynamic shift register which drives the circuit of the next step with other capacitors It is suitable for the circuit which has the circuit which controls a digital circuit like the drive circuit of image sensors, and an analog signal output. It is invention suitable for the circuit by which the dynamic circuit and the ********** circuit were ****ed especially.

[0016] In order to make TFT of high mobility conventionally, to raise the crystallinity of a barrier layer was needed. For that purpose, although it was effective to have raised crystallization temperature to 800 degrees C or more, since the substrate which is equal to use on such conditions will be restrained remarkably, it is not desirable technique. It was discovered that crystallinity improves on the other hand also by setting preferably 70nm or more of the thickness of a barrier layer to 100nm or more. Conversely, 70nm or less of crystallinity of the thickness of a barrier layer was not typically good in a thing 50nm or less.

[0017] It observes that this invention can control crystallinity by such thickness of a barrier layer, and is characterized by obtaining TFT which has a required property with this property on the same substrate.

[0018] For example, by TFT whose thickness of a barrier layer is 100nm, when a barrier layer is crystallized at 550-750 degrees C, although the electric-field mobility of NMOS and PMOS was 2/Vs, and 20-60cm2 / Vs 30-80cm, respectively that whose thickness of a barrier layer is 50nm -- coming out -- the electric-field mobility of NMOS and PMOS fell with 2/Vs, and 5-20cm2 / Vs by 10-30cm, respectively This is in agreement with a difference being in crystallization with the thickness of a barrier layer.

[0019] However, it was discovered by the still interesting thing by such difference in the thickness of a barrier layer that leakage currents also differ. The mode is shown in drawing 1 . In drawing 1 , as for (A), (B) of PMOS shows the property of NMOS, respectively, and b and d whose thickness of a barrier layer of a and c is 100nm show that whose thickness of a barrier layer is 50nm. The direction of TFT whose thickness of a barrier layer NMOS and PMOS is 50nm so that clearly from drawing is the parvus about 1-3 figures from a 100nm thing. According to the research of this invention people, before and after the thickness of a barrier layer was 70nm, as for such an effect, it became clear that change arises very dramatically.

[0020] In TFT as which this invention is a thing using this property, and high mobility is required While setting preferably 70nm or more of the thickness of a barrier layer to 100nm or more, in TFT as which a low leakage current is required rather than mobility the parenchyma from which thickness is different on the same substrate so that 70nm or less may turn into 50nm or less preferably in the thickness of a barrier layer -- the laminating of the genuineness silicon layer is carried out two-layer or more than it, and a thick silicon layer is made into the barrier layer of the former TFT, and let a thin silicon layer be the barrier layer of the latter TFT In this case, to form an insulator layer with a thickness of 100nm or more among these silicon layers is desired. As quality of the material of an insulator layer, oxidization silicon is suitable.

[0021] Instead of forming a two-layer polysilicon contest layer as mentioned above, in a silicon layer, the option of this invention

forms the field in which thickness is different, forms TFT of high mobility in the field where a silicon layer is thick, and forms TFT of a low leakage in a thin field. What is necessary is just to etch alternatively the silicon layer which divided deposition of a silicon layer into two phases, and performed it, or was deposited, in order to change such a silicon layer thickness by the location.
[0022] In this invention, a barrier layer crystallizes the barrier layer of the both sides of high mobility TFT and low leakage-current TFT by heat annealing 450 degrees C or more. Here, heat annealing is used because it excels in homogeneity. In addition, the process of heat annealing does not matter, after forming a gate electrode, or after forming the source/drain.
[0023] The temperature of heat annealing receives a constraint by the material of a substrate or others. When silicon and a quartz are used as a substrate about a constraint of a substrate material, it is possible to a maximum of 1100-degree C heat annealing. For example, in the case of 7059 glass of Corning, Inc. which is a typical alkali free glass, annealing with a temperature of 650 degrees C or less is desirable. However, in this invention, it must be set up in consideration of the property needed for each TFT in addition to a substrate. If an annealing temperature is high, while the crystal growth of TFT will progress and mobility will generally become high, a leakage current increases. Therefore, in order to obtain TFT of the property that it is different on the same substrate like this invention, you should make preferably 450-800 degrees C of the temperature of annealing 550-750 degrees C.
[0024] One example of this invention is setting preferably 70nm or less of the thickness of the barrier layer of TFT of an active matrix field to 10-50nm, and, setting preferably to 100-300nm 70nm or more of the thickness of the barrier layer of TFT used for a circumference circuit on the other hand, using polysilicon contest TFT as a switching transistor, in a part for the display of active matrix circuits, such as liquid crystal.
[0025] In the equipment which has the above display circuit section (active matrix) and its drive circuit (circumference circuit), it is better [****] to make a drive circuit into a CMOS circuit. In this case, as for a transmission gate or an inverter circuit, being CMOS-ized is desirable although all of circuits do not need to be CMOS. The conceptual diagram of such equipment was shown in drawing 2 (A). The active matrix 3 which the data driver 1 and the gate driver 2 are constituted by drawing on an insulating substrate 7, and has TFT in the center section is constituted, and the display to which these driver sections and active matrices were connected by the gate line 5 and the data line 6 is shown. The active matrix 3 is aggregate of the pixel cell 4 which has TFT (a drawing PMOS) of NMOS or PMOS.
[0026] About the CMOS circuit of the driver section, to make preferably concentration of impurities, such as oxygen [barrier layer] and nitrogen for obtaining high mobility, and carbon, or less [1017cm -] into three three or less [1018cm -] is desired. consequently, the threshold voltage of TFT -- NMOS -- 0.5-2V, and PMOS -0.5--3V -- mobility was 2/Vs 20-100cm 30-150cm in NMOS further at 2 / Vs and PMOS
[0027] On the other hand, in the active matrix section, the leakage current could make the small element of about 1 pA small by drain voltage 1V independent or by carrying out and using for two or more serials, and was able to make supplementary capacity unnecessary further completely.
[0028] The 2nd example of this invention is related with the semiconductor memory like DRAM. Semiconductor memory equipment has already reached the limitation of a speed by single crystal IC. Although it is required to enlarge current capacity of a transistor more in order to make the fast turn around beyond this perform, if it not only becomes the cause of one step of increase of the consumed electric current, but cannot expand capacity of a capacitor at all any more about DRAM which performs a storage operation by storing a charge especially in a capacitor, technique only has corresponding by raising a driver voltage.
[0029] Single crystal IC is said that it reached the limitation of a speed because the big loss has arisen with a substrate and the capacity of a wiring in one. If an insulator is used for a substrate and the consumed electric current will not be raised, the drive high-speed enough is possible. Since it is such, IC of SOI (semiconductor of insulating lifter) structure is proposed.
[0030] Also in DRAM, in the case of 1Tr / cellular structure, a previous LCD and previous circuit arrangement are almost the same, and the thickness of the barrier layer of this invention uses preferably 70nm or less of parvus TFT of a 10-50nm leakage current for TFT of the storage bit section also by the other DRAM (for example, 3Tr / cellular structure) of structure. On the other hand, since sufficient fast turn around is needed for the drive circuit, from the purpose for which the thickness of a barrier layer suppresses preferably 70nm or more of power consumption, using 100-300nm TFT, CMOS-izing similarly is desirable [a circuit] like the aforementioned LCD.
[0031] Also in such semiconductor memory equipment, the fundamental block configuration is the same as that of the thing of drawing 2 (A). for example, DRAM -- setting -- 1 -- for a unit storage bit and 5, a bit line and 6 are [a column decoder and 2 / a low decoder and 3 / the storage element section and 4 / a word line and 7] substrates (insulation)
[0032] The 3rd application of this invention is drive circuits, such as image sensors. Although the 1-bit example of a circuit of image sensors was shown in drawing 2 (B), the flip-flop circuit 8 and the buffer circuit 9 in drawing are usually constituted by the CMOS circuit, and the high-speed response which can follow in footsteps of the high-speed pulse impressed to the scanning line is demanded. On the other hand, TFT10 of the signal output stage has undertaken the duty of the dam which emits the charge accumulated by photo diode at the capacitor to the data line with the signal from the shift register sections 8 and 9.
[0033] It is required for such TFT10 a high-speed response and that there are also few leakage currents with last thing. Therefore, in such a circuit, to set preferably 70nm or more of the thickness of the barrier layer of TFT of circuits 8 and 9 to 100-300nm is desired. In one TFT10, it is desired for 70nm or less of the thickness of a barrier layer to be 10-50nm preferably. In this case, it cannot be overemphasized that the thickness of a barrier layer must be optimized so that a leakage current and mobility may agree for the purpose in TFT10.
[0034]

[Example]
[Example 1] this example is shown in view 3 . this example forms polysilicon contest TFT in the circumference circuit and active matrix field of TFT type LCD.
[0035] First, the 1st substratum oxide film 102 was deposited 20-200nm in thickness by the spatter on Corning 7059 substrate 101. Furthermore, the 1st amorphous silicon layer 103 was deposited 30-50nm in thickness on it by the plasma CVD method or reduced pressure CVD which uses a mono silane or a disilane as a raw material. At this time, concentration of the oxygen in an amorphous silicon layer and nitrogen is preferably made or less [1017cm -] into two two or less [1018cm -]. Reduced pressure CVD is suitable for this purpose. In this example, the oxygen density carried out to two or less [1017cm -]. The 2nd oxidization silicon layer (100-150nm in thickness) 104 was again formed by the spatter on this amorphous silicon layer. Furthermore, the 2nd amorphous silicon layer 105 was deposited by the same means. This mode is shown in drawing 3 (A).
[0036] Then, as shown in drawing 3 (B), it left only the circumference circuit field and other 2nd amorphous silicon layer was removed. And the 2nd oxidization silicon layer 104 is removed, using the remaining amorphous silicon layer 106 as a mask, it left the 2nd oxidization silicon layer 107 and the 2nd amorphous silicon layer 106 only to the circumference circuit field, and other fields made the 1st amorphous silicon layer 103 expose after all.
[0037] Furthermore, as shown in drawing 3 (C), the fields 108 (for circumference circuits) and 109 (for matrix TFT) of the shape of an island which forms TFT were formed. And as shown in drawing 3 (D), the gate oxide film 110 was formed by meanses, such as a spatter. Instead of a spatter, TEOS (tetrapod ******** silane) etc. may be used and membranes may be formed by the plasma CVD method. Since the level difference of an island-like field is especially large in this example, although the good membrane formation technique of a step coverage is needed, the membrane formation which used TEOS is suitable for this purpose. However, it is desirable to anneal at the temperature of 650 degrees C or more after the time of membrane formation or membrane formation in this case for 0.5 to 3 hours.
[0038] Then, as shown in drawing 3 (E), the N type silicon layer with a thickness of 200nm - 5 micrometers was formed by the LPCVD method, patterning of this was carried out and the gate electrodes 111-113 were formed in each island-like field. Instead of an N type silicon layer, you may use the metallic materials with comparatively good thermal resistance, such as a tantalum, chromium, titanium, a tungsten, and **********.
[0039] Then, the impurity was poured into the self-matching target into the island-like silicon layer of each TFT by the ion doping method, having used the gate polar zone as the mask. In this case, boron was poured into the left-hand side of the island-like field 108, having covered the right-hand side of the island-like field 108 and the matrix field of drawing by the photoresist after that, and having used [poured in phosphorus, having used the phosphoretted hydrogen (PH3) as doping gas first on the whole surface,] the diboron hexahydride (B-2 H6) as doping gas. Phosphorus set to 2-8x1015cm-2, boron set the dose to 4-10x1015cm-2, and it was set up so that the dose of boron might exceed phosphorus.
[0040] Furthermore, it crystallized by annealing at 550-750 degrees C for 2 to 24 hours. At this example, heat annealing was performed at 600 degrees C for 24 hours. Not only the field where ion was poured in but the barrier layer under the gate electrode which was in the amorphous status till then was also able to be made to crystallize according to this annealing process. However, since the barrier layer of the island-like field 108 was thicker than 100-150nm and the thing (30-50nm in thickness) of the matrix field 109, its former crystallinity was better. Of the above process, the field 114 of P type and the fields 115 and 116 of N type were formed. Sheet resistance of these fields was 200-800ohm/**.
[0041] Then, as shown in drawing 3 (F), the oxidization silicon layer was formed in the whole surface 300-1000nm in thickness by the spatter as a layer insulation object 117. This may be an oxidization silicon layer by the plasma CVD method. Especially by the plasma CVD method which uses TEOS as a raw material, the good oxidization silicon layer of a step coverage is obtained.
[0042] Then, as a pixel electrode 122, by the spatter, ITO layer was formed and patterning of this was carried out. And the contact hole was formed in the source/drain of TFT (impurity range), and the chromium wirings 118-121 were formed. It is shown in drawing 3 (F) that the inverter circuit is formed by left-hand side NTFT and left-hand side PTFT. Wirings 118-121 may be multilayer interconnections with the aluminum which makes chromium or a titanium nitride a substratum, in order to lower sheet resistance. Finally, it annealed at 350 degrees C in hydrogen for 2 hours, and the dangling bond of a silicon barrier layer was reduced. The circumference circuit and the active matrix circuit have been unified and formed according to the above process. Although two kinds of TFT was able to be formed in this example by depositing the two-layer silicon layer with which thickness is different, it is also possible to form the silicon layer with which three kinds of thickness is different similarly, and to form TFT from which three properties are different, and it is also possible to form TFT of much more modalities on the same substrate.
[0043] [Example 2] this example is shown in view 4 . this example forms polysilicon contest TFT in the drive circuit (CMOS logic section and sample & hold (SH) section) of the image sensors using the PIN junction of an amorphous silicon.
[0044] First, the substratum oxide film 202 was deposited 20-200nm in thickness by the spatter on Corning 7059 substrate 201. Furthermore, the amorphous silicon layer 203 was deposited 150-250nm in thickness on it by the plasma CVD method or reduced pressure CVD which uses a mono silane or a disilane as a raw material. At this time, concentration of the oxygen in an amorphous silicon layer and nitrogen is preferably made or less [1017cm -] into two two or less [1018cm -]. Reduced pressure CVD is suitable for this purpose. In this example, the oxygen density carried out to two or less [1017cm -]. And this amorphous silicon layer is etched alternatively and it is the thick field 204 (in the fraction into which it is not etched, thickness is 150-200nm.). it is used for a CMOS circuit -- the thin field 205 (in the fraction into which it was etched, thickness is 30-50nm.) It is used for SH section. It formed. This mode is shown in drawing 4 (A).
[0045] Instead of the technique of using such etching, an amorphous silicon layer with a thickness of 30-50nm is formed first, and

patterning of the photoresist is applied and carried out to this, and further, after depositing a silicon layer 50-170nm in thickness in piles, you may remove the silicon layer of the field by which patterning was carried out by the lift-off method.
[0046] Next, the amorphous silicon layer was crystallized by annealing at 600 degrees C for 24 hours. Then, patterning of these Si layers was carried out to the shape of an island, for example, as shown in drawing 4 (B), the CMOS-circuit field 206 and the TFT field 207 of SH were formed. Furthermore, as shown in drawing 4 (C), these island-like fields were covered, by the spatter, the oxidization silicon layer (50-150nm in thickness) was formed, and this was made into the gate insulator layer 208. Then, the chromium layer with a thickness of 200nm - 5 micrometers was formed by the spatter, patterning of this was carried out and the gate electrodes 209-211 were formed in each island-like field.
[0047] Then, as shown in drawing 4 (D), the impurity was poured into the self-matching target into the island-like silicon layer of each TFT by the ion doping method, having used the gate polar zone as the mask. In this case, boron was poured into the left-hand side of the island-like field 206, and the island-like field 207, having covered only the left-hand side of the island-like field 206 of drawing by the photoresist after that, and having used [poured in phosphorus, having used the phosphoretted hydrogen (PH3) as doping gas first on the whole surface,] the diboron hexahydride (B-2 H6) as doping gas. Phosphorus set to 2-8x1015cm-2, boron set the dose to 4-10x1015cm-2, and it was set up so that the dose of boron might exceed phosphorus.
[0048] Although the crystallinity of a silicon layer was destroyed by the doping process, the sheet resistance can also be considered as a 1kohm/** grade. However, it is possible to reduce sheet resistance more at sheet resistance of this level, by annealing at 600 degrees C further for 2 to 24 hours, in being too large. Moreover, the same descent is obtained also by irradiating the strong light like laser light.
[0049] Of the above process, the field 212 of N type and the fields 213 and 214 of P type were formed. Sheet resistance of these fields was 200-800ohm/**. Then, the oxidization silicon layer was formed in the whole surface 300-1000nm in thickness by the spatter as a layer insulation object 215. This may be an oxidization silicon layer by the plasma CVD method. Especially by the plasma CVD method which uses TEOS as a raw material, the good oxidization silicon layer of a step coverage is obtained.
[0050] Then, the contact hole was formed in the source/drain of TFT (impurity range), and the aluminum wirings 216-219 were formed. It is shown in drawing 4 (E) that the inverter circuit is formed by left-hand side NTFT and left-hand side PTFT. Finally, it annealed at 350 degrees C in hydrogen for 2 hours, and the dangling bond of a silicon layer was reduced. In the drive circuit of image sensors, on the same substrate, it unified simultaneously and the CMOS-circuit field and SH field have been formed according to the above process. What is necessary is just to form an amorphous photoelectric element next, in order to complete image sensors.
[0051]
[Effect of the Invention] this invention was able to solve the technical probrem in the production process of the conventional polysilicon contest TFT by the minimum change used as the barrier layer of TFT of carrying out silicon layer-thickness change so that clearly also from the above explanation.
[0052] this invention was able to raise the reliability and performance of equipment of having a dynamic circuit and such a circuit especially. Although polysilicon contest TFT had low ON/OFF ratio and various distress was in utilization to a purpose like former especially the active matrix of a LCD, it is thought that such a problem was mostly solved by this invention. Furthermore, as shown in the example 2, it can use also for the drive circuit of the image sensors on an insulating substrate. Although an example did not show, it will be clear that an effect can be mentioned by carrying out this invention also in TFT used as a means of solidification of a single crystal semiconductor integrated circuit.
[0053] For example, a circumference logical circuit is constituted from a semiconductor circuit on a single crystal semiconductor, TFT can be prepared through a layer insulation object on it, and this can also constitute the memory device section. in this case -- DRAM circuit which used TFT of PMOS of this invention for the memory device section -- carrying out -- the drive circuit -- a single crystal semiconductor circuit -- CMOS -- it is-izing and constituted And since the memory section will be raised to the second floor when such a circuit is used for a microprocessor, area can be saved. Thus, it is thought that this invention is very useful invention on industry.

[Translation done.]

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2.**** shows the word which can not be translated.
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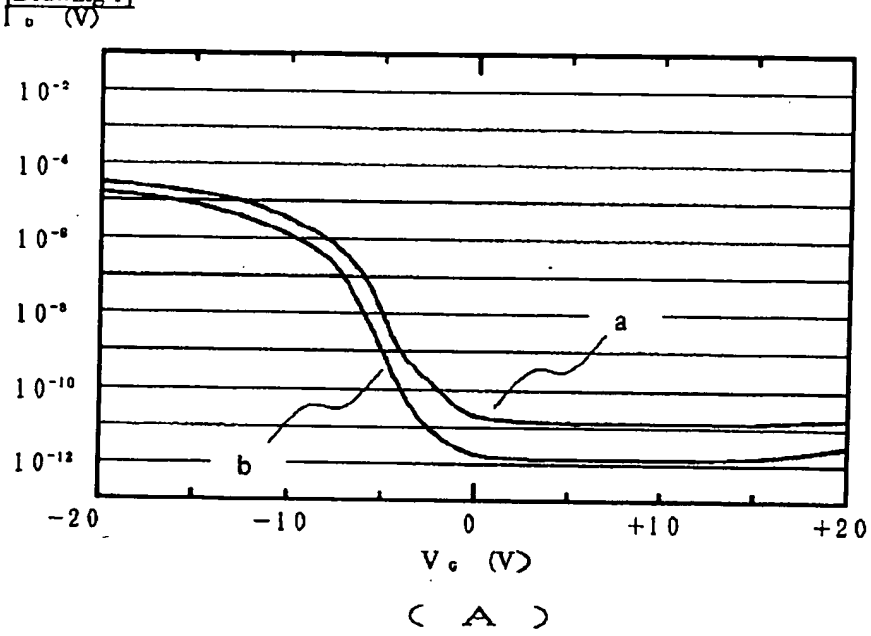
DRAWINGS

[Drawing 1]



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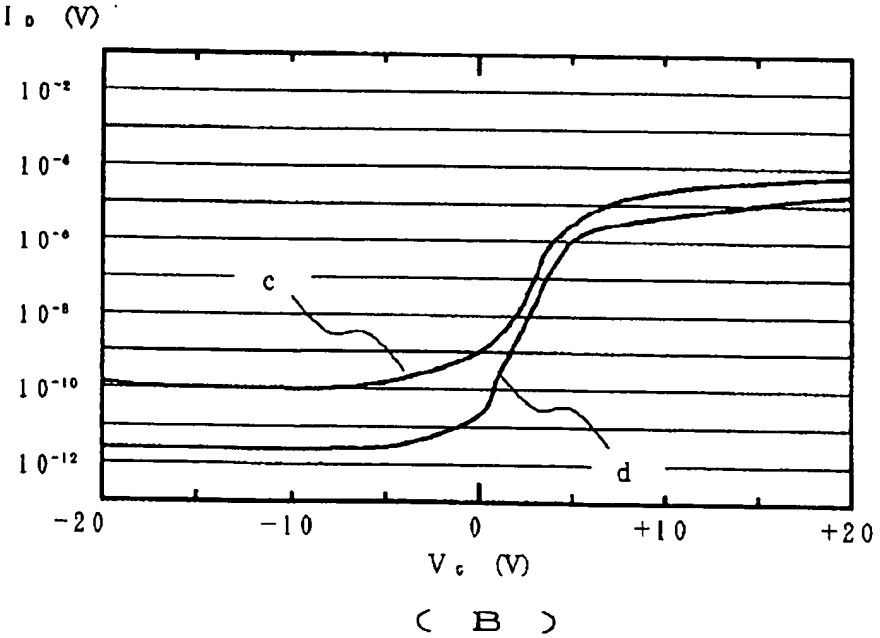
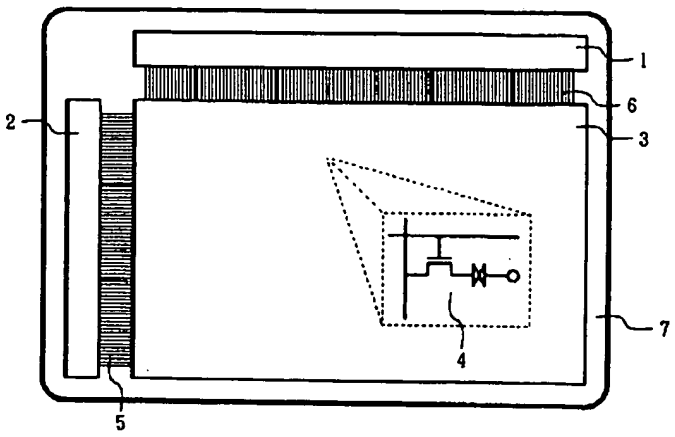


(B)

[Drawing 2]



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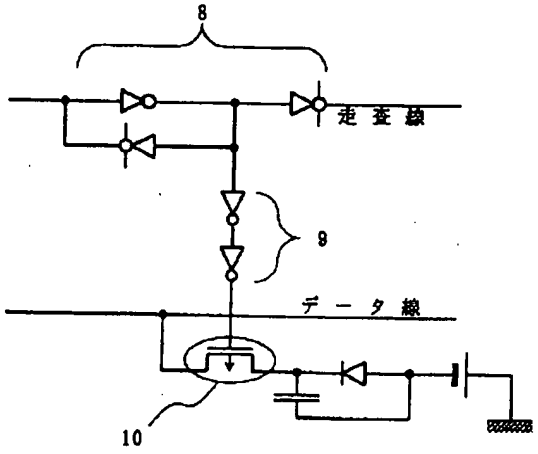
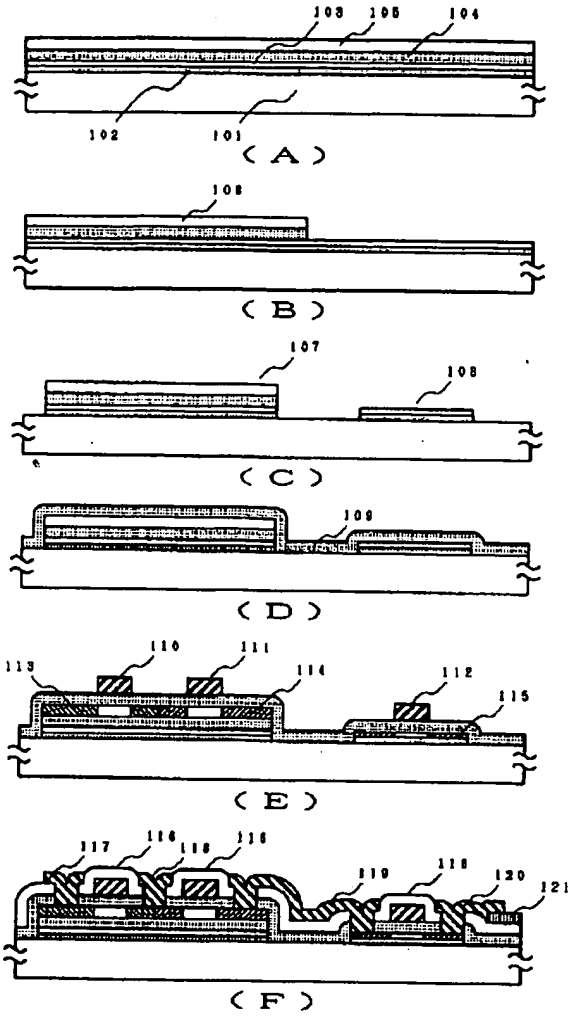


（B）

[Drawing 3]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108
(C)
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(D)
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114
112
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(E)
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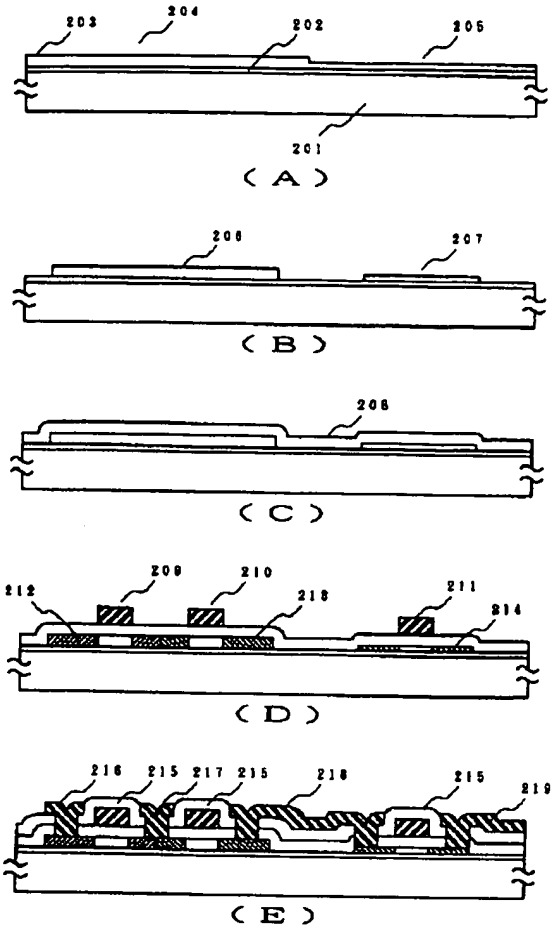
121
(F)

[Drawing 4]



[Translation done.]